FIG. 6A

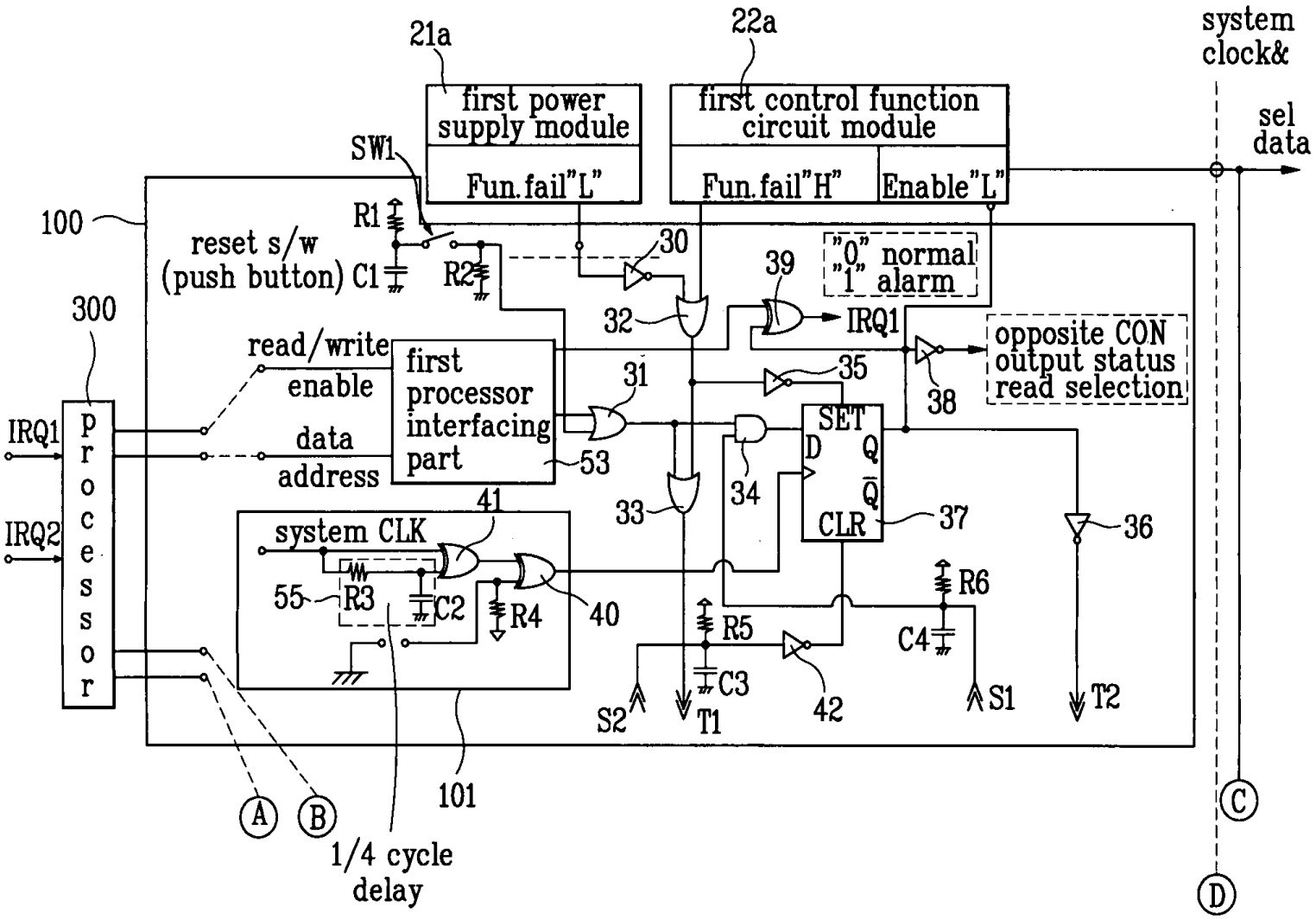

21a
22a
first power supply module
Fun.fail"L"
first control function circuit module
Fun.fail"H"
Enable"L"
system clock&
sel data
SW1
100
R1
reset s/w (push button)
C1
R2
30
39
"0" normal "1" alarm
32
IRQ1
opposite CON output status read selection
38
300
read/write enable
data address
first processor interfacing part
53
31
35
SET
D
Q
CLR
37
34
33
36
IRQ1
IRQ2
processor
41
system CLK
55
R3
C2
R4
40
R5
C3
R6
C4
S2
T1
42
S1
T2
101
A
B
1/4 cycle delay
C
D

FIG. 6B

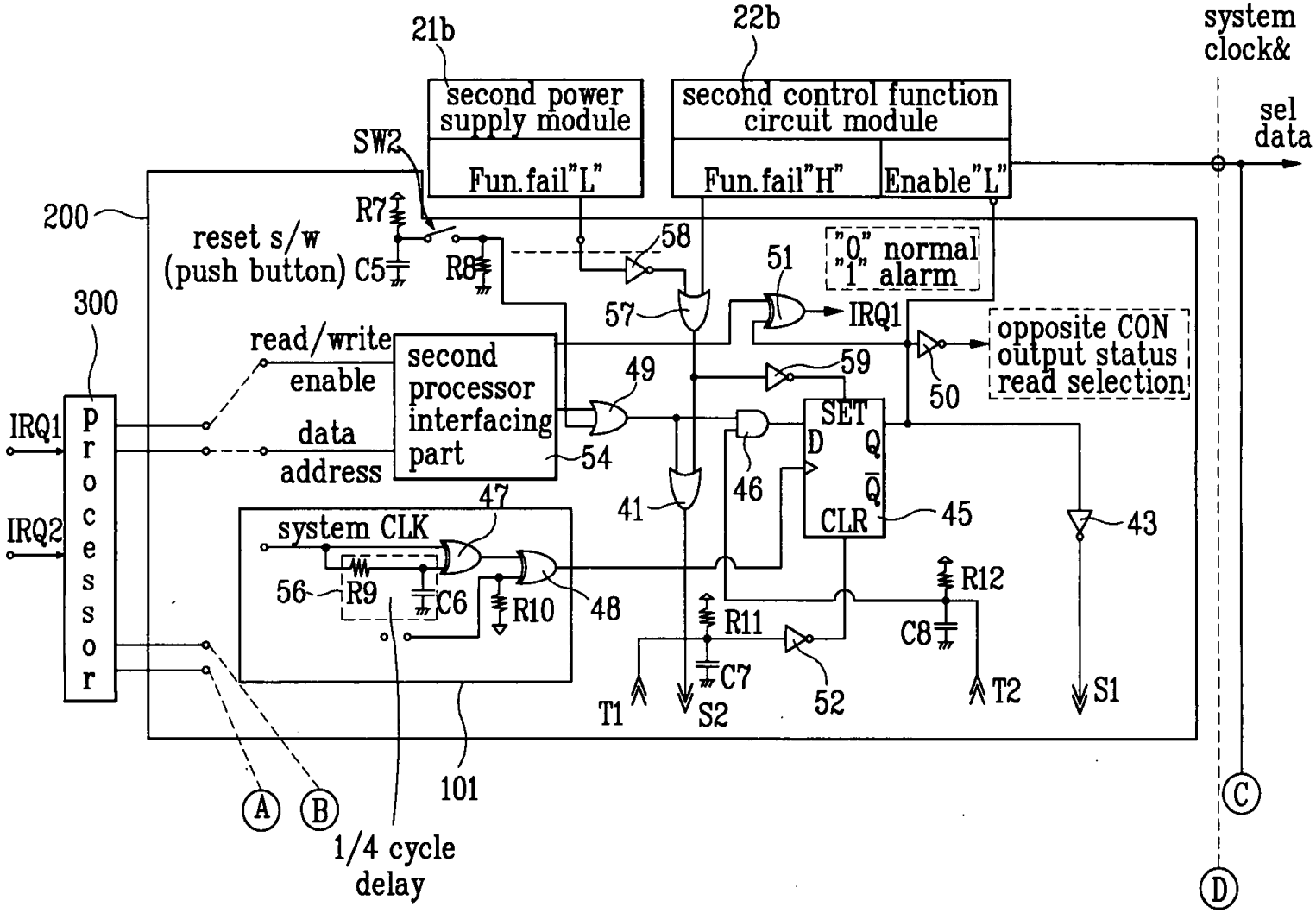
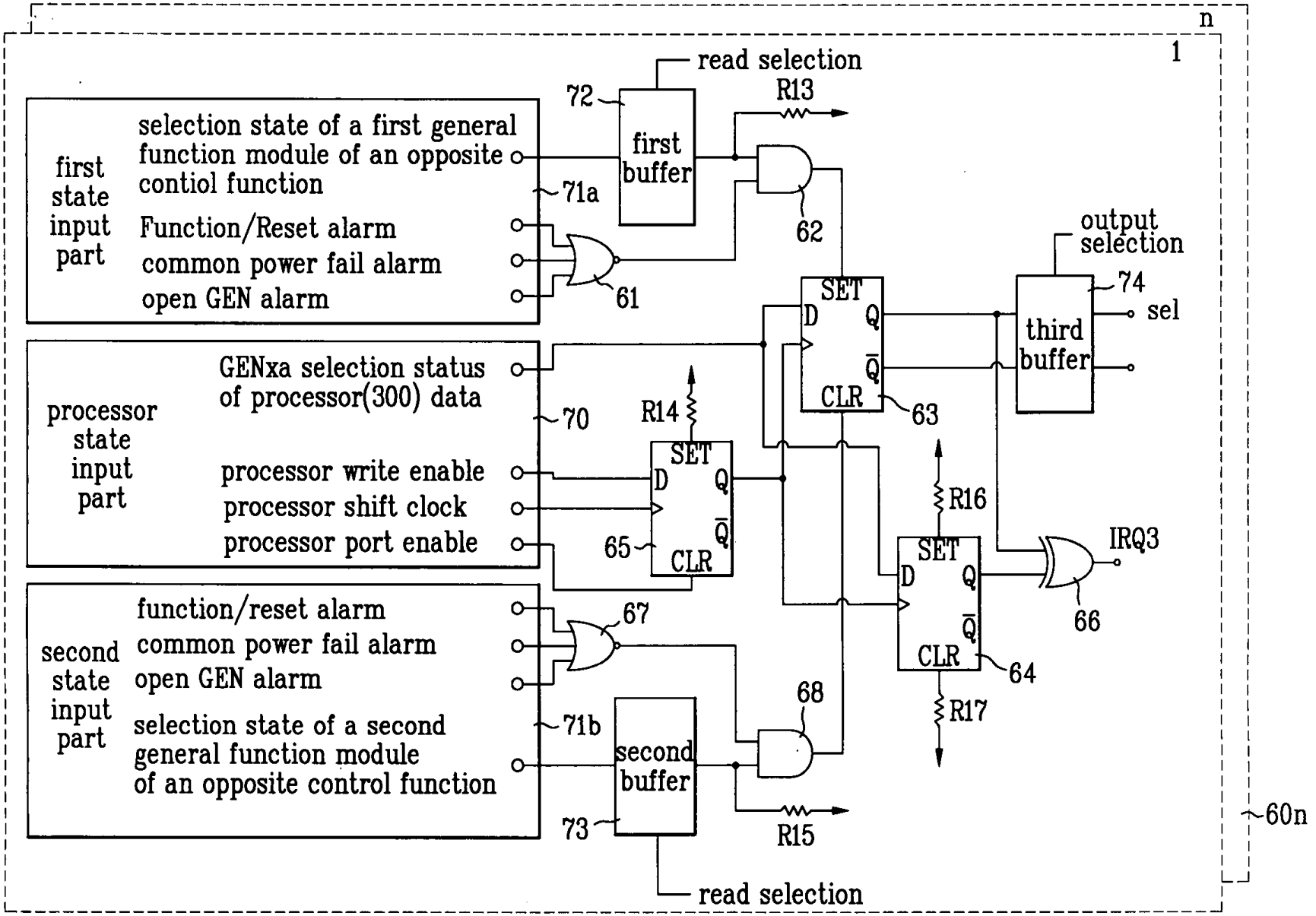

21b
second power supply module
Fun.fail"L"
22b
second control function circuit module
Fun.fail"H"
Enable"L"
system clock&
sel data
SW2
200
R7
reset s/w (push button)
C5
R8
58
51
"0" normal
"1" alarm
57
IRQ1
opposite CON output status read selection
50
59
49
300
read/write enable
data address
second processor interfacing part
54
IRQ1
IRQ2
Processor
41
46
SET
D
Q
CLR
45
43
47
system CLK
56
R9
C6
R10
48
R12
C8
R11
C7
T1
S2
52
T2
S1
101
A
B
1/4 cycle delay
C
D

FIG. 7


n
1
read selection
R13
72
first buffer
selection state of a first general function module of an opposite contiol function
first state input part
Function/Reset alarm
common power fail alarm
open GEN alarm
71a
61
62
output selection
74
sel
third buffer
SET
D
Q
CLR
63
GENxa selection status of processor(300) data
processor state input part
70
R14
processor write enable
processor shift clock
processor port enable
65
R16
IRQ3
66
64
R17
function/reset alarm
common power fail alarm
open GEN alarm
second state input part
67
68
71b
selection state of a second general function module of an opposite control function
second buffer
73
R15
read selection
60n